RF Local Oscillator Path for GSM Direct Conversion Transceiver with True 50% Duty Cycle Divide by Three and Active Third Harmonic Cancellation

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Abstract — **An RF local oscillator frequency path for a multi-band GSM direct conversion transceiver is described that makes use of a novel true 50% output duty cycle divide by 3 circuit and provides active third harmonic cancellation through means of phase recombination of the divider's outputs.**

I. Introduction

The local oscillator (LO) path in a communication system provides the mixing tone to up convert low frequency modulated signals in the transmitter and to down convert received signals so that they may be demodulated. On channel LO frequencies can interact with and corrupt received and transmitted signals, forcing the use of an off channel LO. A way to avoid this is to divide the LO frequency by three and then to double or quadruple it. This guarantees that neither the LO nor any of its harmonics correspond to the received or transmitted frequency.

II. The LO in Direct Conversion Receivers

There are several ways in which an on channel LO can degrade performance in a direct conversion radio. In the case of the receiver, if the LO signal is at the same frequency as the RF, interactions can lead to DC offsets which would corrupt data in modulation schemes such as EDGE or GSM [1] which contain information at DC. These DC offsets can also overwhelm cascaded high gain baseband stages and saturate them. LO to RF interactions can also take the form of the LO signal coupling to the LNA inputs and mixing itself down. Similarly, strong out of band signals present at the antenna and amplified by the LNA can couple onto the LO and modulate it. Such an effect generates spurs on the LO that can mix down the very unwanted signal that generated them, resulting in a baseband output that is difficult to distinguish from the wanted signal.

Interactions of both types can be reduced by use of offset frequency schemes. One method for generating offset LO signals is through the use of a combination of frequency dividers and multipliers. It is generally advisable in such a scheme that any subharmonic LO present be of even order relative to the transmitted or received frequency. Differential hard switched LO chains and mixers tend to generate odd harmonics of the switching frequency. Hard-switched circuits also respond to interfering signals close to their odd harmonics as if they were sidebands of the fundamental. In other words, an LO running at an odd subharmonic of the RF will tend to both radiate and be modulated by the RF, obviating the use of an offset LO.

Possible implementations of on chip VCOs also restrict the choice of LO frequency range. VCOs designed to run at frequencies between 1 and 2GHz [2] are relatively common, whereas lower frequency oscillators are difficult to implement with on chip inductors due to Q limitations and higher frequency designs tend to lose tuning range due to parasitic capacitance and require more power. Although these restrictions are by no means absolute, they do favor the use of an odd order frequency division followed by an even order frequency multiplication and a VCO frequency in the range of 1 to 2GHz. For quad band GSM, the scheme that fits these requirements is shown in Fig. 1.

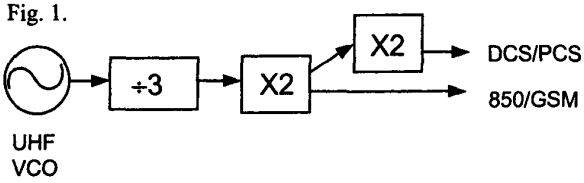

Fig. 1. Chain using a UHF VCO with f_c = 1350MHz to generate quad band LO.

Although this fixed ratio frequency offset LO scheme prevents most UHF VCO to RF interactions, it still is vulnerable to harmonic interactions. For example in the 3/2 LO scheme, if the divide by three circuit generates strong second harmonics at its output, these harmonics correspond to the original RF frequency that one is trying to avoid. Similarly, a non 50% duty cycle LO is much

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more sensitive to pick up of RF signals and their harmonics. Hence it is desirable to use dividers and multipliers that are as harmonically clean as possible in the LO path.

III. Frequency Doubling and Polyphase Filters

Frequency doubling can be accomplished by multiplying two 90° phase split signals together. The doubling function falls out from equation (1).

$$\text{Sin}(\omega t)*\text{Cos}(\omega t)=1/2*\text{Sin}(2\omega t) \quad (1)$$

An efficient doubling circuit actually makes use of tuned output loads and hard switched phase split signals in the place of sinusoidal ones. A circuit such as the one shown in Fig. 2 accomplishes frequency doubling.

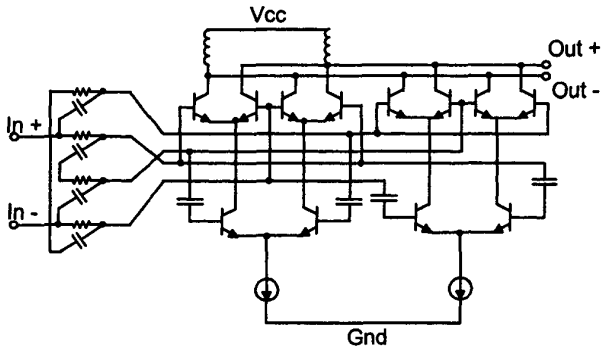

Fig. 2. Low harmonic doubler.

The quadrature phase split is provided by an RC polyphase filter. The resulting signal then drives a pair of hard-switched Gilbert multipliers [3]. The use of two such multipliers, whose outputs are summed and whose inputs are cross-coupled, provides higher order symmetry [4]. This symmetry guarantees low even order harmonics provided that the phase split is accurate. A tuned load is used to reduce any odd order harmonics that may be present at the output.

Polyphase filters are commonly used to provide quadrature phase splits in LO chains. Their capacity for providing accurate phase splits without requiring any frequency division combined with their passive nature (implying high linearity, low noise, and low power consumption) make them ideal for many designs.

There is a constraint placed on the allowable input harmonic content associated with the use of polyphase filters when they are followed by hard-switched circuits. The primary issue with RC polyphase filters arises from their frequency dependent output amplitude matching. In hard switched LO chains, this is typically not a problem for the fundamental frequency, since the hard switched nature of the LO chain provides a degree of amplitude independence. If the stage immediately preceding a polyphase generates significant harmonics, and the stage immediately following it is hard switched (as in the case of the frequency doubler discussed above), significant phase errors can result (Fig. 3).

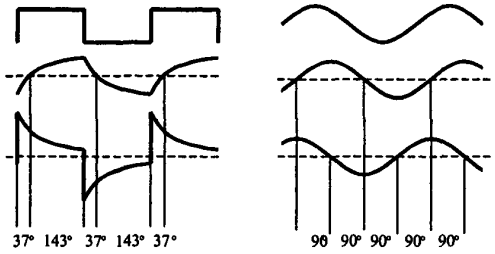

Fig. 3. Polyphase response to square wave and sinusoidal inputs. Effective phase of zero crossings marked.

This effect is a consequence of harmonics being unevenly distributed between the outputs, offsetting their zero crossings. It is therefore desirable that the stages that drive polyphase filters have outputs that are as spectrally pure as possible.

IV. Low Harmonic Divide By Three

The first circuit that follows the UHF VCO in the LO path divides the UHF frequency by 3. As explained above, this is required to ensure non-harmonic frequency isolation between the RF and UHF frequencies. Traditional divide by 3 circuits suffer from a few shortcomings. The foremost amongst these is the fact that the output signals are typically rich in even order harmonics. This high harmonic content results from outputs taking the form of rectilinear waveforms with non 50% duty cycles.

Since the output waveforms of a typical frequency divider are derived only from the rising edges of its input, odd order divider outputs are typically restricted to pulse widths that are integer multiples of the period of their inputs. Since a full output cycle of an odd order divider is equal to an odd number of its input cycle, getting a 50% output duty cycle requires pulse widths that correspond to a non integer number of input cycles. In order to generate 50% duty cycle outputs, one would need a structure that could transition on both rising and falling edges of the

input (assuming a 50% duty cycle at the input). We demonstrate exactly such a structure here. The key is the use of a specialized level triggered D flip-flop. Such a flip flop takes as its inputs D, CLK, and an additional input θ, which sets the polarity of the CLK signal that triggers it. The truth table of such a flip-flop is shown in Table 1.

D	θ	CLK	Q
0	0	0	0
0	0	1	Hold
0	1	0	Hold
0	1	1	0
1	0	0	1
1	0	1	Hold
1	1	0	Hold
1	1	1	1

Table 1. Truth table for polarity switchable flip flop

A divide by N, with a 50% duty cycle can be implemented with a ringed arrangement incorporating N of the specialized level triggered flip-flops. This holds true even in the case where N is an odd integer. By dynamically driving the θ inputs of the flip flops, the outputs can be made to transition on either a rising or falling edge, depending on the state of other flip flops in the circuit. Each flip flop's output drives the next one's input, with an inversion in the feedback. The θ input of each flip-flop receives its input from the flip-flop that follows it. The actual implementation of the divide by 3 circuit used is shown in Fig. 4.

It can be seen that if a given flip flop clocks in a high

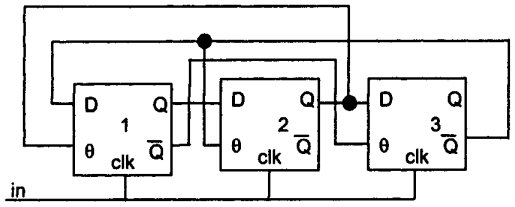

Fig. 4. Architecture of divide-by-3 frequency divider with 50% duty cycle.

signal on a positive edge, once that signal has been passed on to the next flip flop, it will start clocking on the negative edge of the clock. See Fig. 5a.

In order for a divider to provide symmetrical outputs

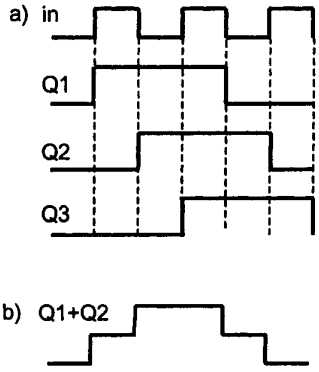

Fig. 5a) Internal states of divide-by-3
5b) Output, generated by two internal states

free of 2nd order harmonics, it is important that it be symmetrical. Also, since it is desirable that all signals, inverted or not, propagate with the same delay, a fully differential topology is needed. Hence the flip-flops have been implemented using emitter-coupled logic (ECL) (see Fig. 6).

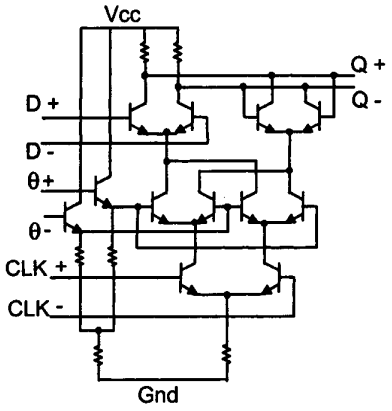

Fig. 6. Phase switchable ECL D Flip Flop

Essentially this design is a standard ECL level triggered D flip flop, but with an extra set of switching pairs between the clock input and the cross coupled bistable memory stage. Phase inversions are accomplished simply by swapping the differential signal.

One additional benefit of this design provides becomes clear when looking at the waveforms generated within the divider. The three differential, internal waveforms are phase split by 60°. By taking a combination of two of

these as an output, an interesting effect is seen (see Figure 5b). While the fundamentals add almost in phase with each other (their sum is lower than the maximum possible) the 3rd harmonics are 3*60°=180° out of phase and so cancel (Fig. 7). As a result, the output is spectrally clean up to the fifth harmonic, where filtering is relatively easy. This provides the desired sinusoidal input to the frequency doubler's polyphase filter.

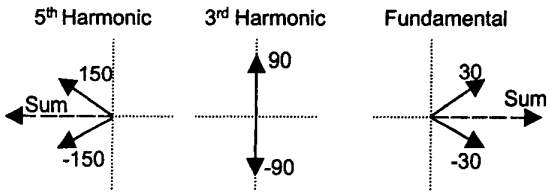

Fig. 7. Phasor diagram demonstrating 3rd harmonic cancellation in summed 60° split square waves.

V. Measured Results.

It has been difficult to directly measure the performance of this LO path, as it is part of a fully integrated transceiver (Fig. 8) [7]. Performance must therefore be inferred from receiver and transmitter measurements. The divider works at input (UHF VCO) frequencies as high as 1750MHz. The divider core consumes 8mW from a 2.7V supply. The recombination buffer, which cancels the third harmonic and drives the succeeding polyphase filters also consumes 8mW at 2.7V.

The output phase noise floor of the divider is lower than -153dBc/Hz$^{1/2}$. The doubler, which is only on in DCS and PCS modes, consumes 16mW and provides an output

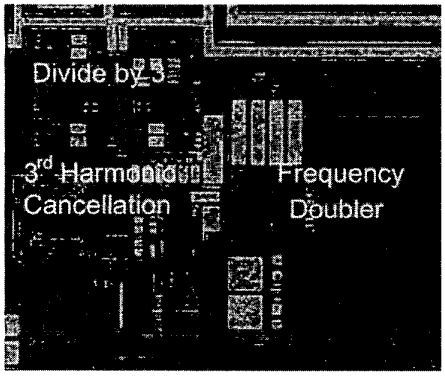

Fig. 8. Microphotograph of frequency divider and doubler circuit

noise floor of less than -147dBc/Hz$^{1/2}$. A measure of the overall performance of this LO architecture is in the amount of on frequency LO present at the LNA input. In GSM mode, only -110dBm is detected (at 915MHz) as compared to the +10dBm of power in the UHF VCO core (at 1395MHz), thus giving an effective isolation of 120dB.

VI. Conclusion

An offset LO scheme for use in direct conversion radio transceivers has been presented. To avoid unwanted interactions between the LO and RF signals, the circuits have been designed to generate a minimum of even order harmonics. To accomplish this, a divide by three circuit incorporating polarity switchable ECL flip-flops was developed to provide true 50% duty cycle outputs. Additionally, a particular combination of the phased outputs of such a divider suppresses the third harmonic providing a spectrally clean signal. Such a signal is ideal for driving polyphase filters incorporated in frequency doublers and quadrature mixers.

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